REMARKS

This application has been carefully reviewed in light of the Office Action dated December 27, 2007. Claims 1, 3 to 7, 20, 22 to 26 and 39 remain in the application, of which Claims 1, 20 and 39 are independent. Reconsideration and further examination are respectfully requested.

Claims 1, 3, 7, 20, 22, 26 and 39 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,488,673 (Katayama), and Claims 4 to 6 and 23 to 25 were rejected under § 103(a) over Katayama in view of U.S. Patent No. 6,977,756 (Nakano). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention aims to reduce the necessary memory for processing image data. According to claim 1, the buffer can be reduced since the quantization component quantizes the integral portion of the corrected image data, and the buffer stores the calculated quantization error. Note that the quantization of the integral portion of the corrected image data results in an arithmetic error. Thus the arithmetic error should be compensated. To accomplish this, the bit connection component connects a decimal portion of image data of a preceding pixel to image data of a target pixel as lower bits of the image data of the target pixel. Note that the decimal portion corresponds to lower bits and the integral portion corresponds to upper bits.

Referring specifically to the claims, amended independent Claim 1 is directed to an image processing apparatus comprising a bit connection component that connects a decimal portion of image data of a preceding pixel to image data of a target pixel as lower bits of the image data of the target pixel, a correction component that generates corrected image data by adding a correction value to the bit-connected image

data of the target pixel, a latch component that latches a decimal portion of the corrected image data to be connected to image data of a next pixel, a quantization component that quantizes an integral portion of the corrected image data, a calculation component that calculates the quantization error, which is generated by quantization by the quantization component, a buffer that stores the calculated quantization error, and an error diffusion component that generates the correction value to be added to input data of the next pixel by diffusing the quantization error stored in the buffer.

Claims 20 and 39 are method and computer medium claims, respectively, that substantially correspond to Claim 1.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of Claims 1, 20 and 39, and in particular, is not seen to disclose or to suggest at least the features of a bit connection component (step) that connects a decimal portion of image data of a preceding pixel to image data of a target pixel as lower bits of the image data of the target pixel, a correction component (step) that generates corrected image data by adding a correction value to the bit-connected image data of the target pixel, and a quantization component (step) that quantizes an integral portion of the corrected image data.

Katayama is seen to focus on compensation of arithmetic error generated by error diffusion. To achieve this object, Katayama proposes adding error data to pixel data of an objective pixel, and binarizing the sum of the error data and the pixel data of the objective pixel, calculating distribution error (integral portion), which is generated in the binarization, and distributing the error to appropriate neighboring pixels. Finally, the total sum of the truncated decimal portions is distributed to neighboring pixels. In addition,

referring to Fig. 25 of Katayama, it is found that an arithmetic error computing means 905 and an arithmetic error distributing means 906. An error storing means 908 stores an arithmetic error of decimal portion computed by the arithmetic error distributing means 906. However, the quantization part of Kayayama is not a component that quantizes the integral portion of the corrected image data. Therefore, Katayama cannot provide the benefit of reducing the buffer.

Nakano is not seen to make up for the deficiencies of Katayama. Nakano is seen to disclose that a data driven type processing device has an error diffusion computing unit built therein. An error holding register is provided within the error diffusion-computing unit, and is used to successively store and update a value of error information of a pixel that is to be diffused to a neighboring pixel being processed continuously. An error data memory is provided outside the computing unit, and is used to store and update a value of the error information that is to be diffused to another neighboring pixel being processed discontinuously. The error information and the values to be diffused are stored in a packet, and the packet is circulated for operation. However, Nakano is not seen to disclose or to suggest anything that, when combined with Katayama, would have resulted in at least the features of a bit connection component (step) that connects a decimal portion of image data of a preceding pixel to image data of a target pixel as lower bits of the image data of the target pixel, a correction component (step) that generates corrected image data by adding a correction value to the bit-connected image data of the target pixel, and a quantization component (step) that quantizes an integral portion of the corrected image data.

Thus, Claims 1, 20 and 39, as well as the claims dependent therefrom, are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

/Edward Kmett/

Edward A. Kmett
Attorney for Applicants
Registration No.: 42,746

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3800
Facsimile: (212) 218-2200

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